

Getting Started with MicroSim

Click on the icon for the topic you want to learn more about.



MicroSim's Family of Products



Evaluation CD-ROM Limits



MicroSim Documentation



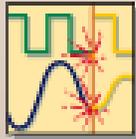
What's New for Release 8.0

How To Get Started

Click on the icon for the topic you want to learn more about.



Using MicroSim Schematics



Using MicroSim PSpice A/D



Using MicroSim PCBoards



Using MicroSim PLSyn



Using MicroSim DesignLab



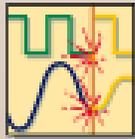
click



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Using MicroSim Schematics



Using MicroSim PSpice A/D



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Using MicroSim PLSyn



Using MicroSim FPGA



click

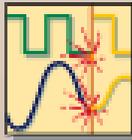


Evaluation CD-ROM Limitations

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MicroSim Schematics



MicroSim PSpice A/D



MicroSim PCBboards



click

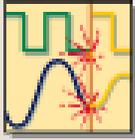


MicroSim Schematics Limitations

- ➔ Schematic capture limited to one schematic page (A-size).
- ➔ Maximum of 25 symbols can be placed on a schematic.
- ➔ Maximum of nine symbol libraries can be configured.
- ➔ Maximum of 20 symbols in a user-created symbol library.
- ➔ Sample library includes 22 analog and 140 digital parts.



click



MicroSim PSpice A/D Limitations

- ➔ **Circuit simulation limited to circuits with up to:**
 - ★ **64 nodes**
 - ★ **10 transistors**
 - ★ **2 operational amplifiers**
 - ★ **65 digital primitive devices, or a combination thereof**
 - ★ **10 ideal transmission lines with not more than four non-ideal lines (lossy lines using RLGC parameters) and four coupled lines**

- ➔ **Device characterization limited to diodes.**

- ➔ **Stimulus generation limited to sine waves (analog) and clocks (digital).**



click



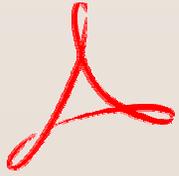
MicroSim PCBs Limitations

- ➔ Limited to 4 signal layers; 50 nets
- ➔ Limited to 30 components per layout
- ➔ Limited to 34 specific footprints:

199D/C/A1	199D/E/E	2ck05	ck06	DIP4
DIP6	DIP8	DIP14	DIP16	DIP18
DIP24	DO-35	DO-41	EDGE26	JLCC84
LCC84	R2012	R3216	RC05	RC07
RC20	SIP5	SO14	SO16	TO-18
TO-39	TO-92	TO-204A	TO-220AB	TO-247AB
DSHELL09-M-90		HDR20	Jump1	Jump2



click



MicroSim Documentation

MicroSim documentation is available in both hardcopy and online formats.

- ★ **MicroSim Schematics User's Guide**
- ★ **MicroSim PSpice A/D & Basics+ User's Guide**
- ★ **MicroSim PSpice & Basics User's Guide**
- ★ **MicroSim PSpice A/D Reference Manual** (this manual is online only)
- ★ **MicroSim PSpice Optimizer User's Guide**
- ★ **MicroSim PLSyn Programmable Logic Synthesis**
- ★ **MicroSim PCBoards User's Guide**
- ★ **MicroSim PCBoards Reference Manual** (this manual is online only)
- ★ **MicroSim PCBoards Autorouter User's Guide**
- ★ **MicroSim Application Notes** (this manual is online only)
- ★ **Library List** (this manual is online only)



Go to books



click



What is MicroSim FPGA?

- ➔ Used to design Xilinx FPGAs (Field Programmable Gate Arrays).
- ➔ Part of MicroSim DesignLab and works with MicroSim Schematics for design entry, and MicroSim PSpice A/D for simulation.
- ➔ Includes Xilinx Universal Library with symbols for XC2000, XC3000, XC4000, XC4000E, XC5200 device families, including XBLOX .
- ➔ Only PC-based tool that can integrate FPGAs into your overall mixed analog/digital system design.

*Only from
MicroSim*

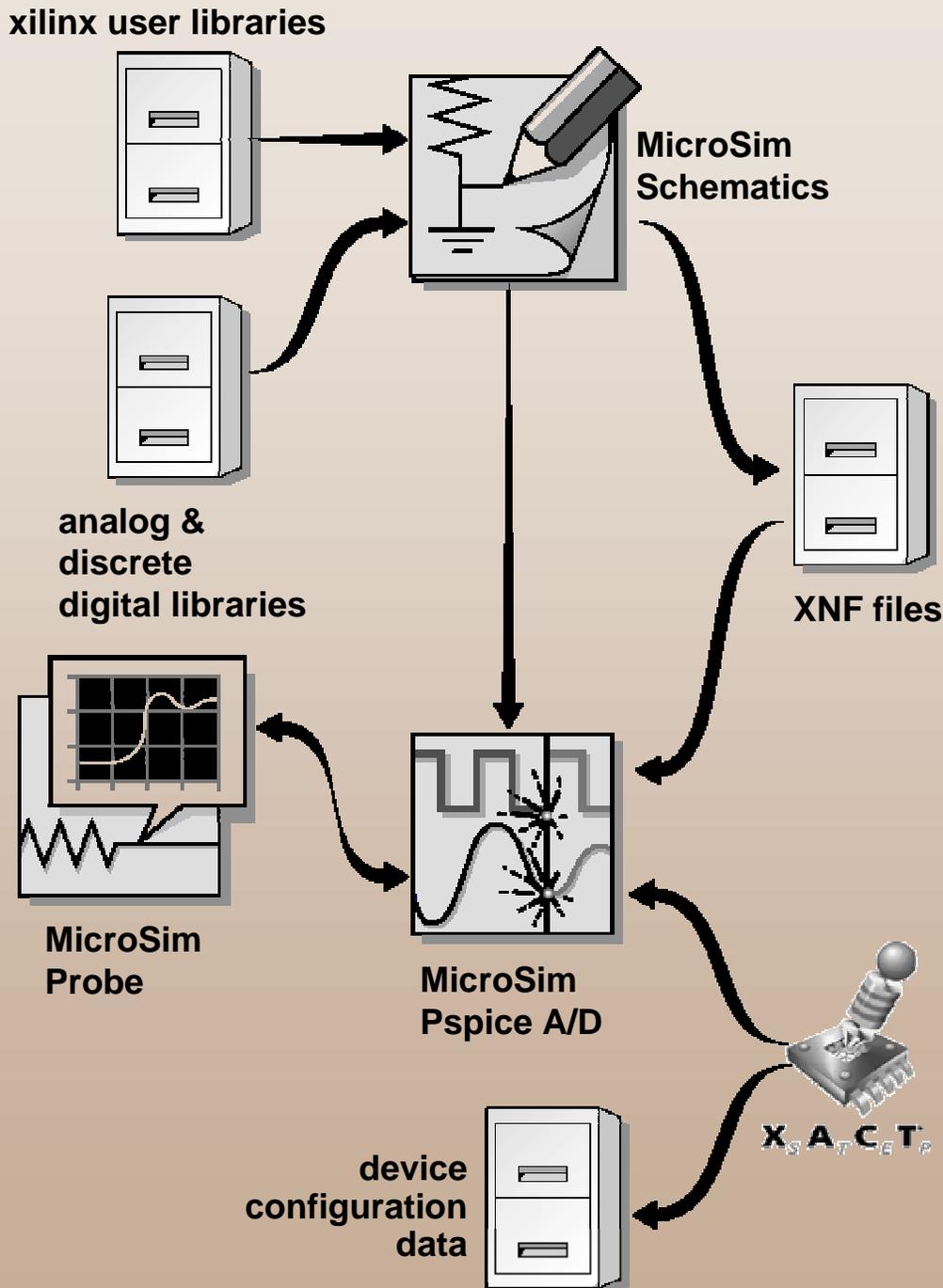


What is it Used For?

- ★ **Creating** integrated designs combining FPGAs with analog and discrete digital devices.
- ★ **Designing** stand-alone FPGAs.
- ★ **Performing** functional simulation (before place and route).
- ★ **Performing** timing simulation (after place and route).
- ★ **Accessing** Xilinx XACTstep from MicroSim Schematics.

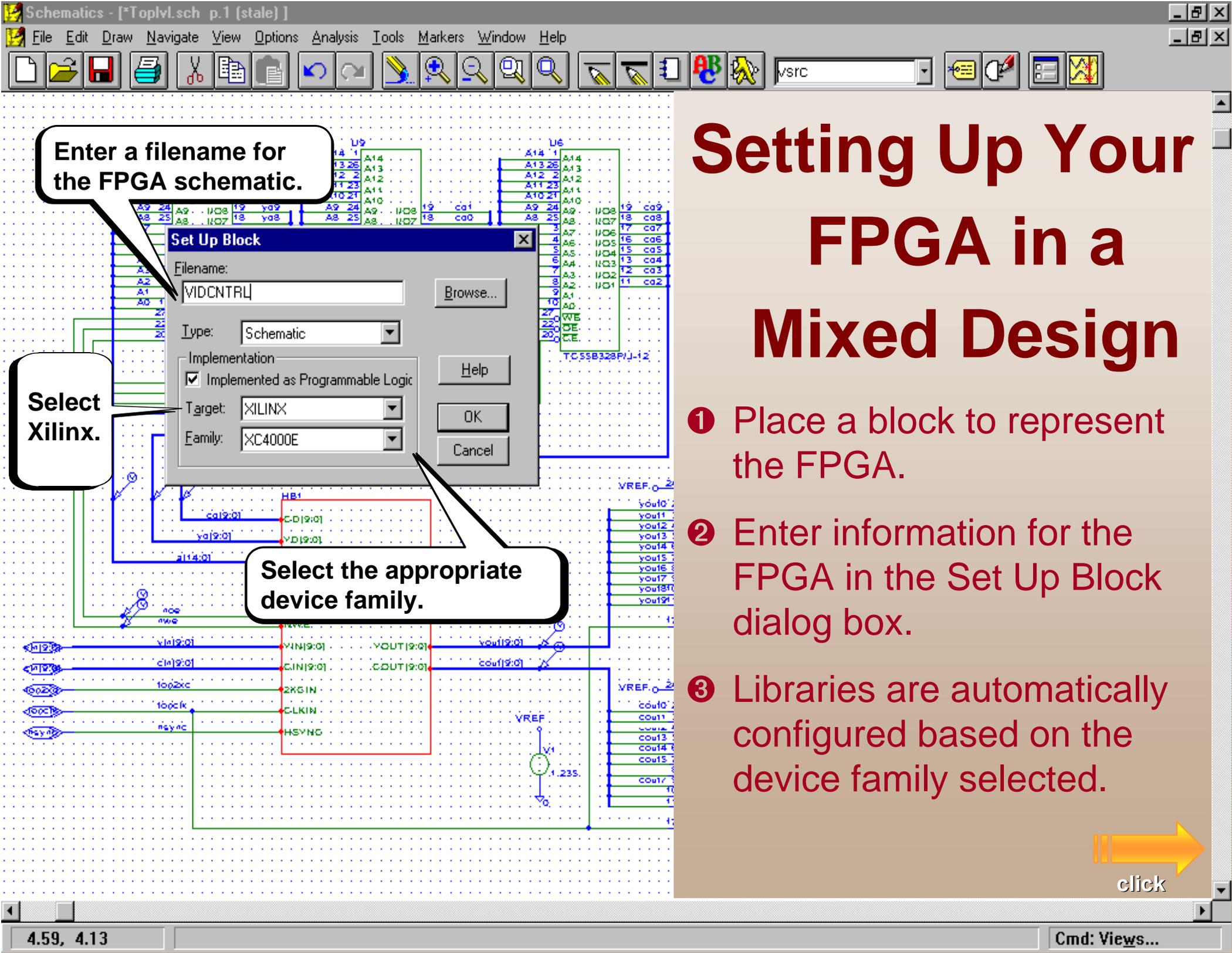


Using MicroSim FPGA



- 1 Design entry in MicroSim Schematics.
- 2 Functional simulation and analysis of simulation results in MicroSim Probe.
- 3 Placing and routing in Xilinx XACTstep.
- 4 Timing simulation and analysis of simulation results in Probe.





Enter a filename for the FPGA schematic.

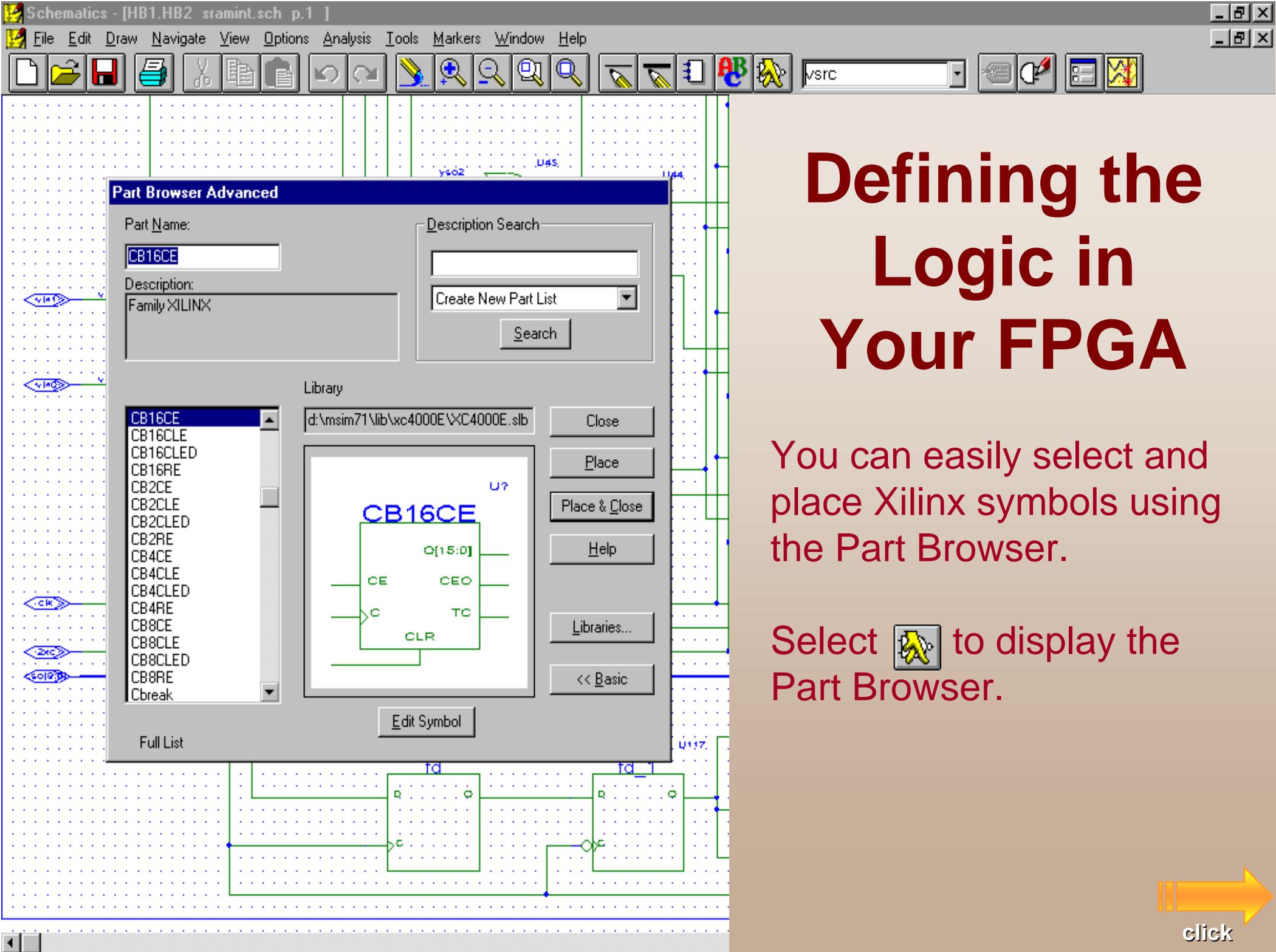
Select Xilinx.

Select the appropriate device family.

Setting Up Your FPGA in a Mixed Design

- 1 Place a block to represent the FPGA.
- 2 Enter information for the FPGA in the Set Up Block dialog box.
- 3 Libraries are automatically configured based on the device family selected.





Defining the Logic in Your FPGA

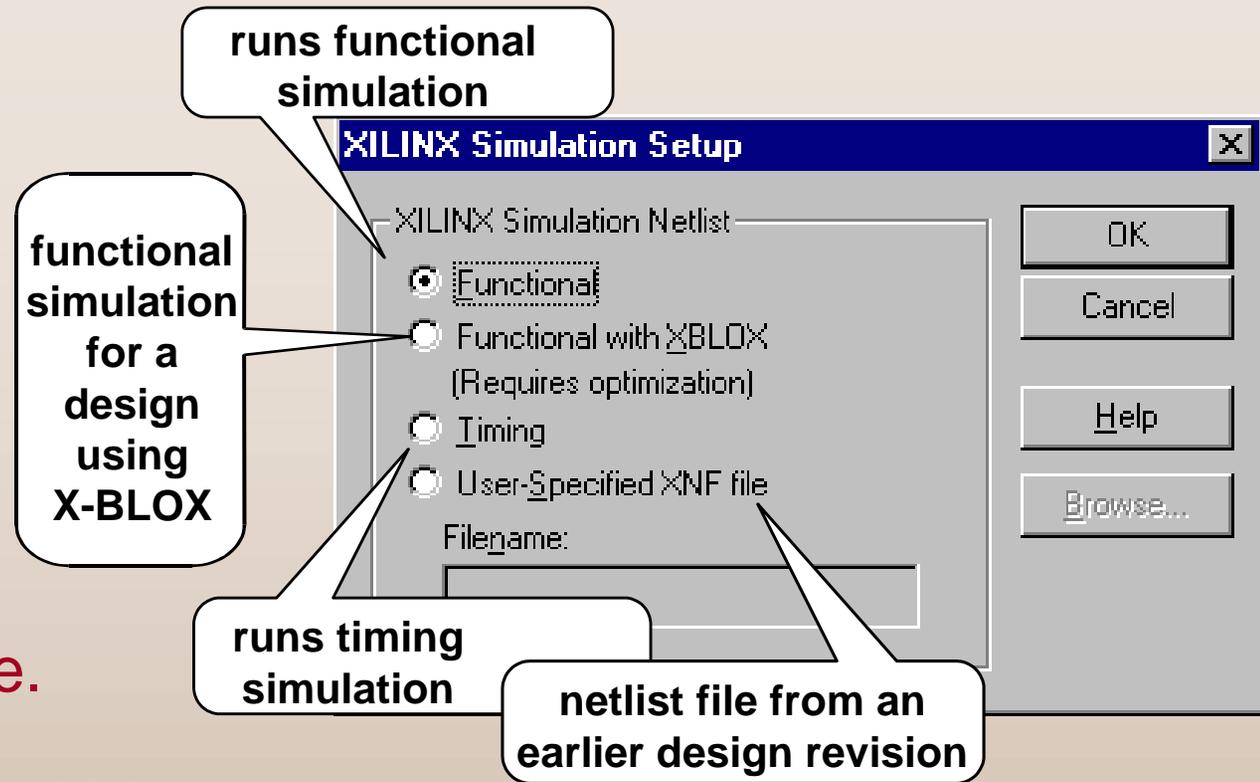
You can easily select and place Xilinx symbols using the Part Browser.

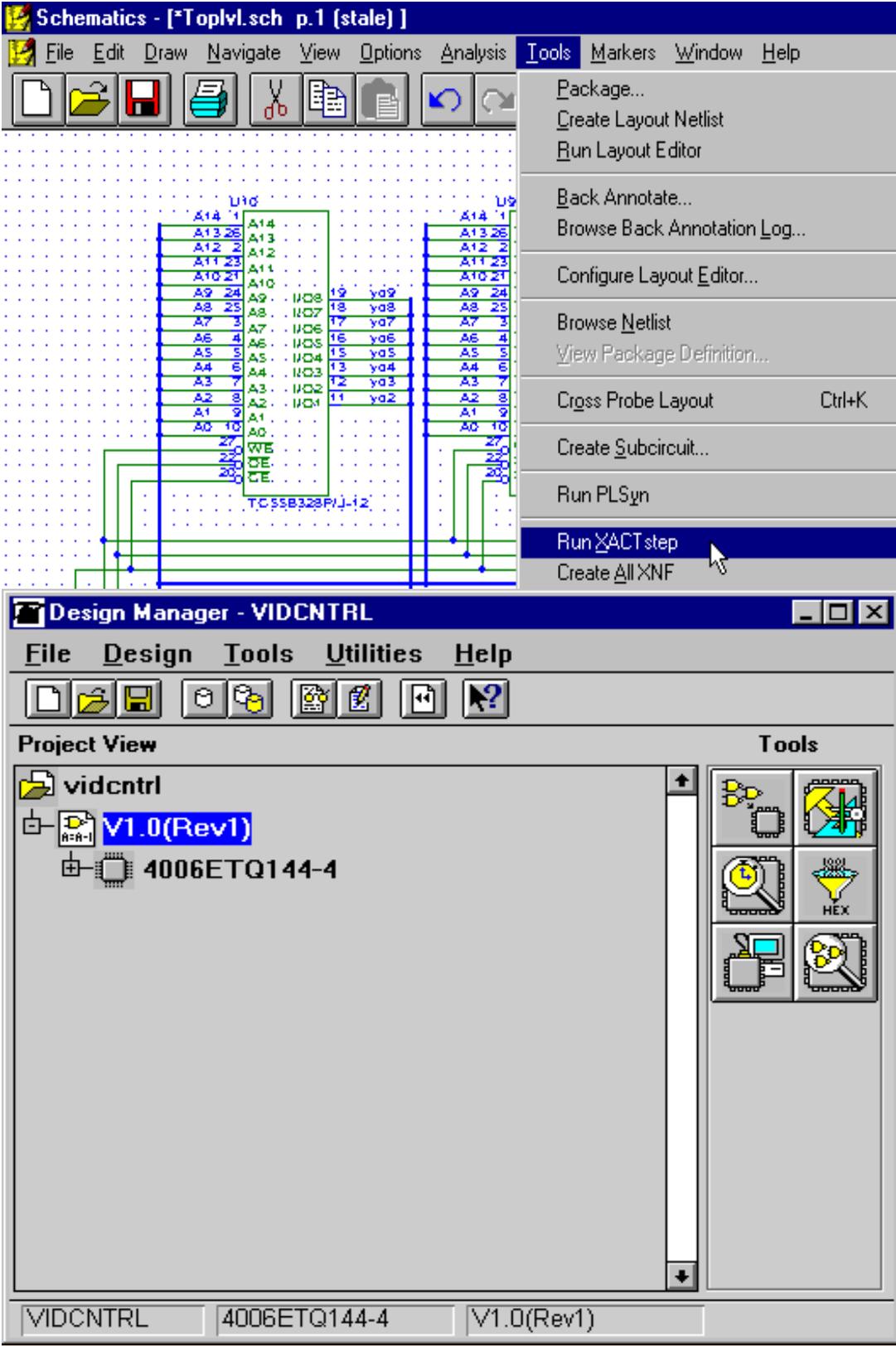
Select  to display the Part Browser.



Functional Simulation

- ★ Use functional simulation to quickly debug designs prior to place and route.
- ★ For mixed designs, you can simulate the entire design or the FPGA only.
- ★ Easy simulation setup—select functional simulation in the Simulation Setup dialog box, then start simulation.
- ★ View simulation results in Probe.

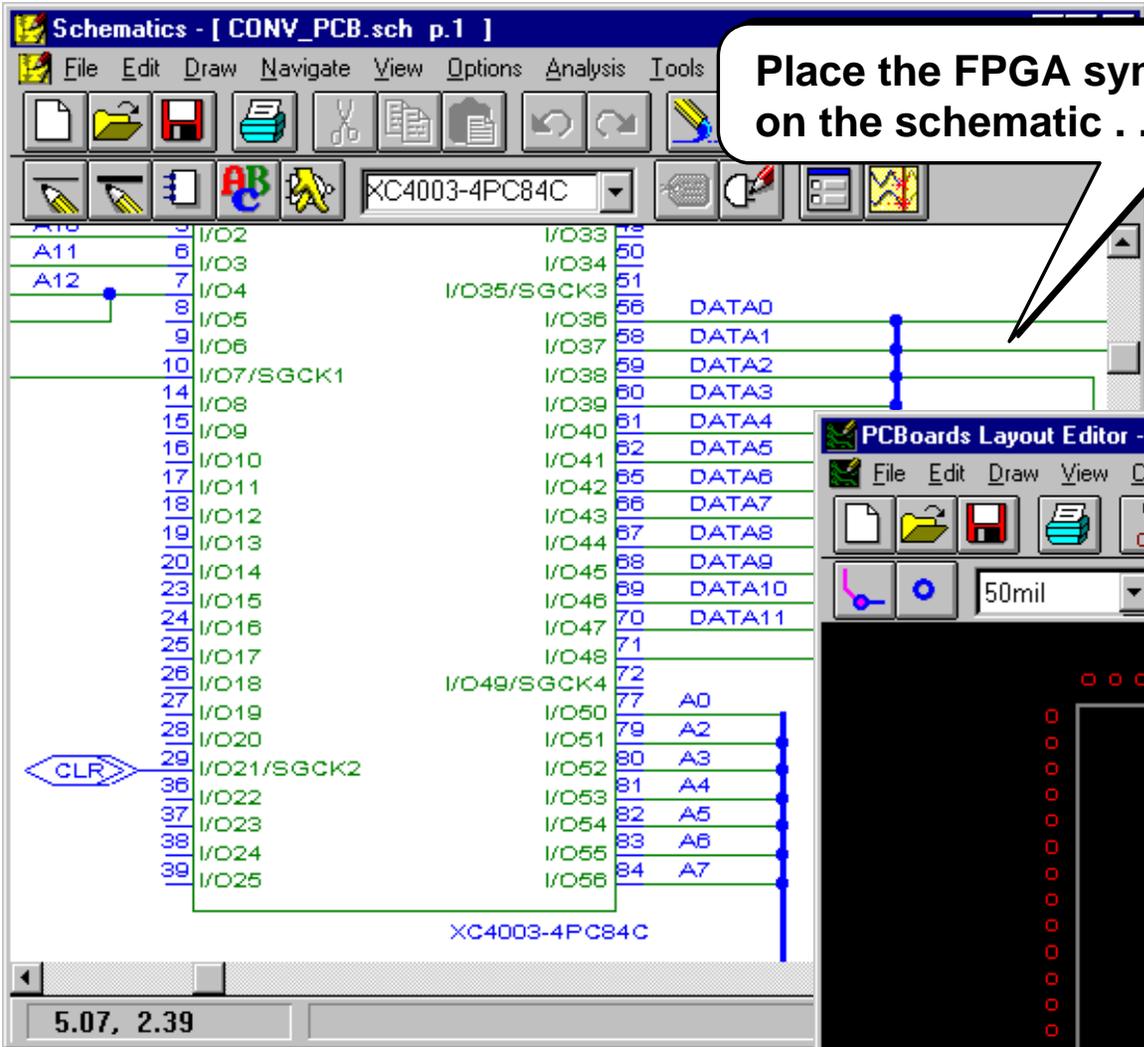




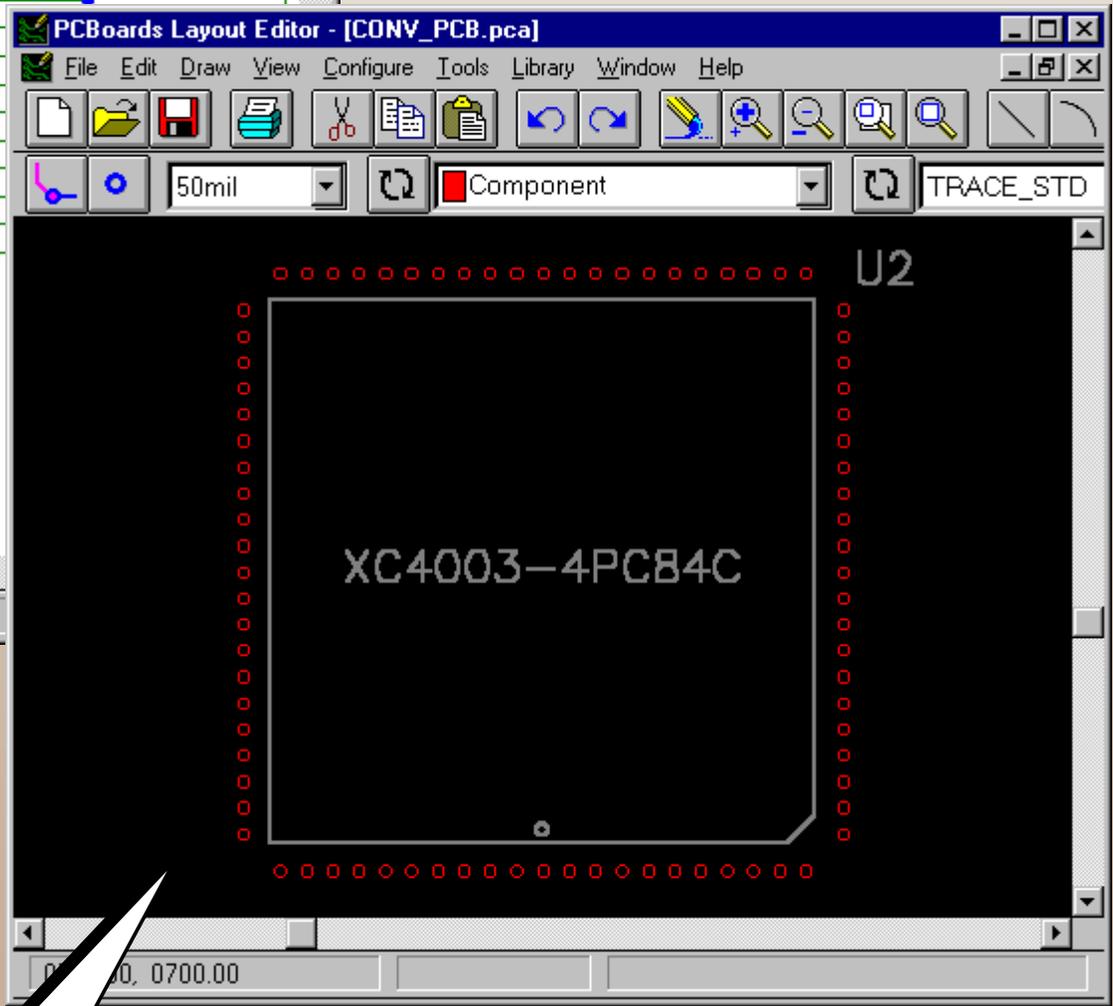
Running Xilinx XACTstep

- ➔ Running XACTstep from Schematics is easy—just select Run XACTstep from the Tools menu.
- ➔ Each time you run XACTstep, XNF files are automatically updated as needed.





Preparing for PCB Layout



FPGA, symbol, package and footprint libraries are included.

... then lay out the board in MicroSim PCBoards.



MicroSim FPGA

Bring accurate circuits to market faster!

Only from
MicroSim

- ➔ Only PC-based tool that integrates FPGAs with analog and discrete digital devices in a complete system design.
- ➔ Integrated simulation: access both functional and timing analysis through Schematics.
- ➔ Quick access to XACTstep.





What is the MicroSim PSpice Optimizer?

The MicroSim PSpice Optimizer is a circuit optimization program that improves the performance of analog and mixed analog/digital circuits. With the PSpice Optimizer, you can:

- ★ Run optimizations
- ★ Explore performance tradeoffs
- ★ Fit model parameters



click

What is it Used For?

Running optimizations

The PSpice Optimizer performs iterative simulations, while adjusting the values of design parameters until performance goals, subject to specified constraints, are nearly or exactly met.

Exploring performance tradeoffs

The PSpice Optimizer provides graphical feedback showing performance. You can also tweak goal and constraint values to examine changes to parameter values.

Fitting model parameters

Given a parameterized model, a set of measured data points, and a good starting point for the parameter values, the PSpice Optimizer fits a more accurate model.

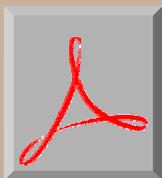


click

Using the PSpice Optimizer

The PSpice Optimizer is fully integrated with other MicroSim programs. This means you can:

- ★ Design your circuit with MicroSim Schematics.
- ★ Simulate with MicroSim PSpice A/D (or MicroSim PSpice).
- ★ Analyze results with MicroSim Probe.
- ★ Optimize performance within the same environment.



PSpice Optimizer
User's Guide

click



click



Using MicroSim PCBboards

You can use MicroSim PCBboards to:

- ★ **Specify printed circuit board structure as well as the components, metal and graphics required for fabrication.**
- ★ **Produce the artwork used in the manufacturing process, including information about the electrical and physical characteristics of the PCB layout.**



click

Starting MicroSim PCBboards

Start MicroSim PCBboards by doing one of the following:



In Schematics, from the Tools menu, select Run PCBboards.



From the Start menu, point to the MicroSim program group, then select the MicroSim PCBboards icon.



Starting a New Layout

Start a layout using one of four methods:

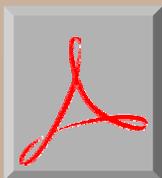
- ★ Load a netlist (MicroSim Schematics or PADS-compatible) into a default layout.
- ★ Load a netlist (MicroSim Schematics or PADS-compatible) into a structured layout (template concept).
- ★ Modify an existing layout and rename it.
- ★ Place components and connections interactively (on-the-fly).



Loading a Netlist

Netlist files contain a collection of component and connectivity declarations, and provide a convenient method for loading the layout.

- ★ **MicroSim Schematic netlist (.nlf) describes the parts and connectivity as defined in the functional design created in Schematics.**
- ★ **PADS netlist (.pad) describes the parts and connectivity of a design in the PADS-compatible format generated by other schematic capture and layout programs.**



click

**PCBoards
User's Guide**



click

What is MicroSim PLSyn?

- ➔ Used to design PLDs (Programmable Logic Devices) and CPLDs (Complex PLDs).
- ➔ Works with MicroSim Schematics and MicroSim PSpice A/D.
- ➔ Includes a part library with up to 3,500 PLDs and CPLDs from 12 manufacturers: Altera, AMD, Atmel, Cypress, ICT, Lattice, and more!
- ➔ Allows mixed-mode (schematic and language) design entry.
- ➔ Automatically partitions your design into multiple devices (with the PLSyn Partitioning option).
- ➔ Only PC-based tool that can integrate PLDs and CPLDs into your overall mixed analog/digital system design.

*Only from
MicroSim*

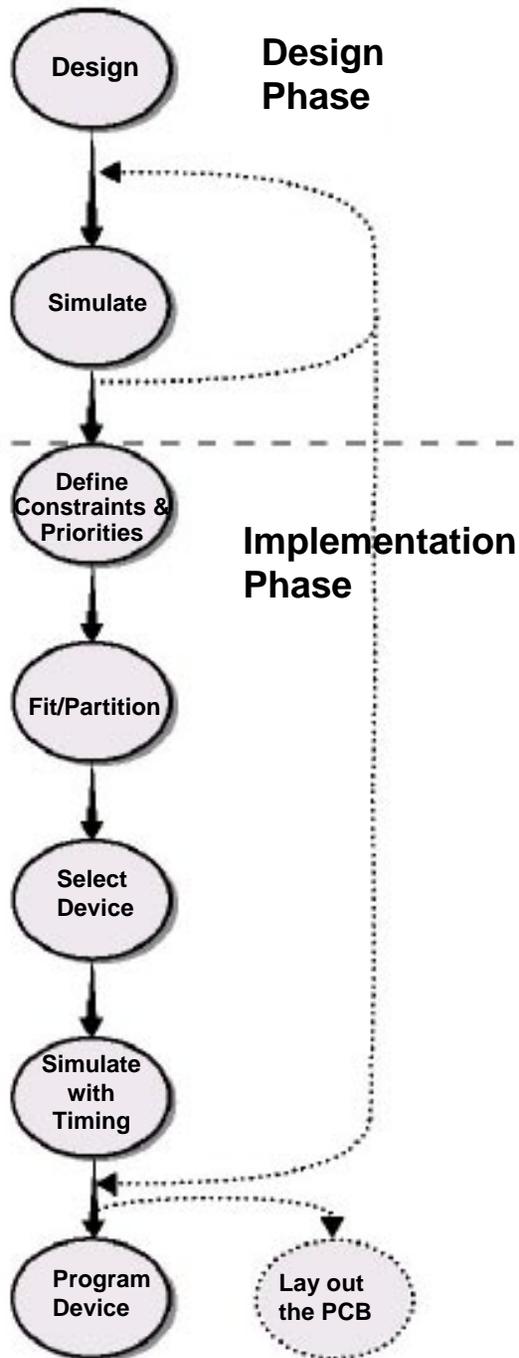


What is it Used For?

- ★ **Creating** integrated designs combining PLDs and CPLDs with analog and discrete digital devices.
- ★ **Generating** a list of device solutions that meet your design specifications; you then select the configuration that best fits your design.
- ★ **Performing** functional simulation (before fitting and part selection).
- ★ **Performing** timing simulation (after part selection).
- ★ **Generating** fuse map files.



Using MicroSim PLSyn



- 1 Enter your design in Schematics.
- 2 Perform functional simulation, and analyze simulation results in Probe.
- 3 Set device constraints and priorities.
- 4 Run the PLSyn fitter to create a list of device solutions; solutions can be a single device or multiple devices (with the Partitioning option).
- 5 Select a solution to implement your design.
- 6 Perform timing simulation, and analyze simulation results in Probe.
- 7 Generate fuse maps to program the PLDs and/or CPLDs in your design.



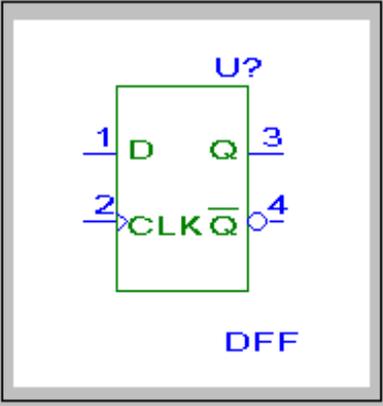
Part Browser Advanced

Part Name: Description Search:
Description: D-type flip-flop Create New Part List

Library: c:\msim71\lib\dig_prim.slb

DFF
DFFC
DFFCR
DFFCRH
DFFCRS
DFFCRSH
DFFCS
DFFCSH
DFFR
DFFRH
DFFRS
DFFRSH
DFFS
DFFSH
DH0006
DH0006C
DH0006CH

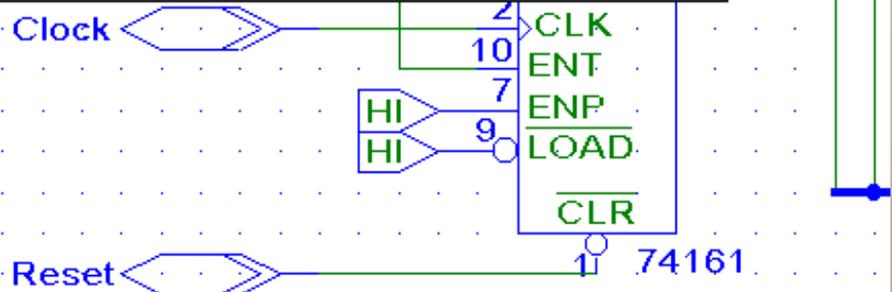
Full List



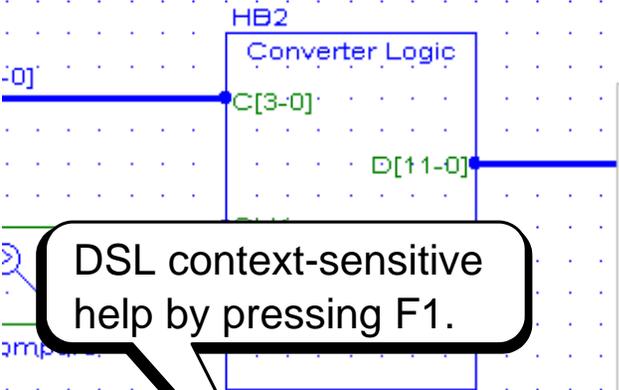
Placing Logic Symbols in Your Design

You can easily select and place logic symbols with the Part Browser.

Use generic (e.g., gates or flip-flops), or 7400 Series logic symbols.



Placing DSL Blocks in Your Design



```
sa_cntrl.dsl* - MicroSim Text Editor
File Edit Search View Insert Help

PROCEDURE SAPR(
  INPUT C1k, Cmp, C[3..0];
  OUTPUT D[11..0] CLOCKED_BY C1k DEFAULT_TO LAST_VALUE);

" Control logic for successive approximation AtoD converter

CASE C
  WHEN 0 => D = 100000000000b; "start with msb
  WHEN 1 => D[10] = 1; D[11] = Cmp;
  WHEN 2 => D[9] = 1; D[10] = Cmp;
  WHEN 3 => D[8] = 1; D[9] = Cmp;
  WHEN 4 => D[7] = 1; D[8] = Cmp;
  WHEN 5 => D[6] = 1; D[7] = Cmp;
  WHEN 6 => D[5] = 1; D[6] = Cmp;
  WHEN 7 => D[4] = 1; D[5] = Cmp;
  WHEN 8 => D[3] = 1; D[4] = Cmp;
  WHEN 9 => D[2] = 1; D[3] = Cmp;
  WHEN 10 => D[1] = 1; D[2] = Cmp;
  WHEN 11 => D[0] = 1; D[1] = Cmp;
  WHEN 12 => D[0] = 0; D[1] = Cmp;
END CASE;

END sapr;
```

Enter blocks of DSL (Design Synthesis Language) to specify logic for your design.

DSL context-sensitive help by pressing F1.

MicroSim PLSyn Help

File Edit Bookmark Options Help

Contents Index Back Print << >>

DSL CASE Statement

Syntax CASE *expression*
 WHEN *value_or_range* =>
 statements
 [ELSE
 statements]
END CASE;

Term	Description
<i>value_or_range</i>	a single value, a list of values, or a range of numbers to which <i>expression</i> is compared
<i>statements</i>	one or more statements. If the <i>expression</i> matches the <i>value_or_range</i>

Insert Template

Available DSL templates:

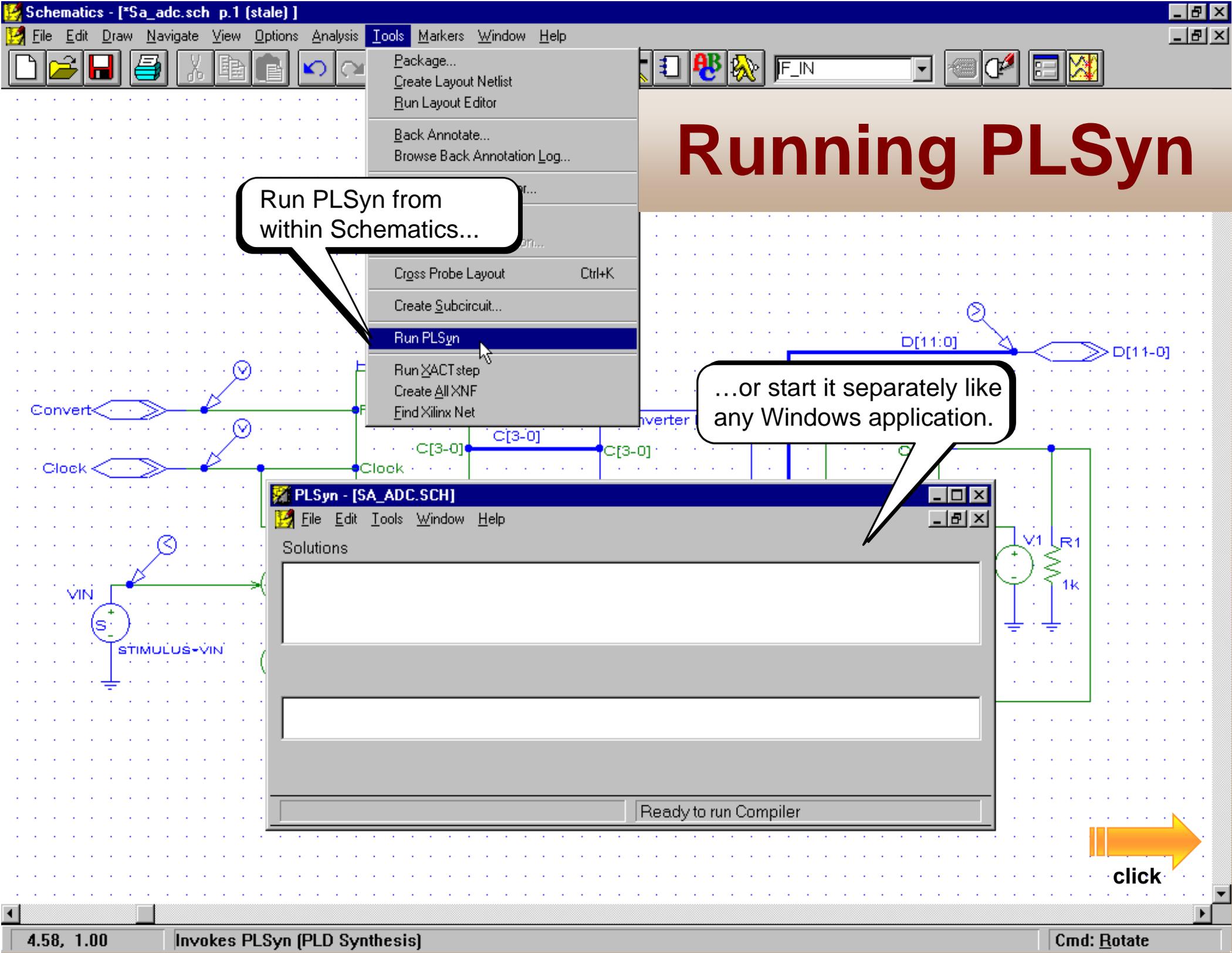
- CASE
- D_FLOP (w/preset)
- D_FLOP (w/reset)
- D_FLOP (w/reset and preset)
- D_LATCH (w/preset)
- D_LATCH (w/reset)
- D_LATCH (w/reset and preset)
- FUNCTION
- IF
- IF-THEN-ELSE
- INCLUDE
- JK_FLOP (w/preset)
- JK_FLOP (w/reset)
- JK_FLOP (w/reset and preset)

Buttons: Insert, Cancel, Help

MicroSim Text Editor

Insert pre-defined DSL "templates."





Running PLSyn

Run PLSyn from within Schematics...

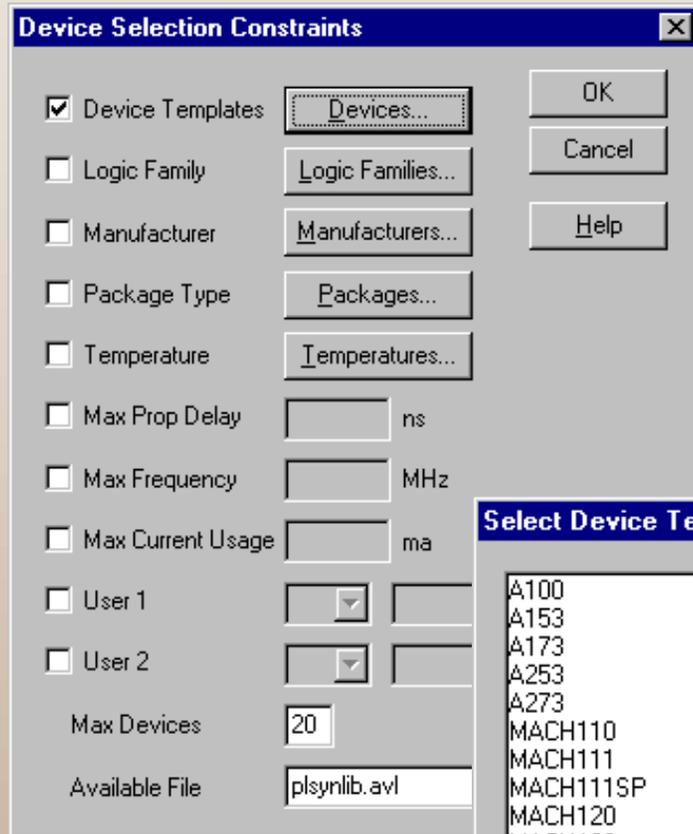
...or start it separately like any Windows application.



click

Setting Constraints

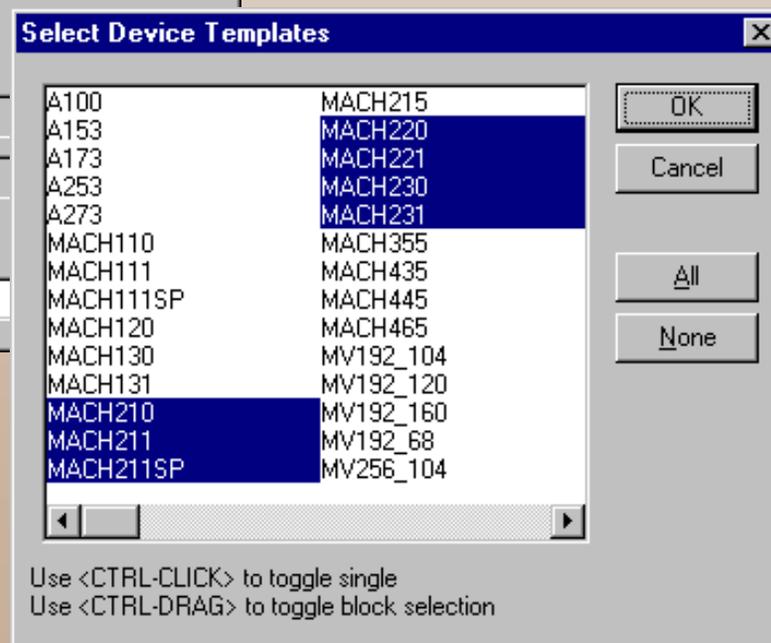
Use constraints to narrow the list of devices that the PLSyn fitter considers when searching for solutions to your logic design.



The 'Device Selection Constraints' dialog box contains the following options:

- Device Templates (with a 'Devices...' button)
- Logic Family (with a 'Logic Families...' button)
- Manufacturer (with a 'Manufacturers...' button)
- Package Type (with a 'Packages...' button)
- Temperature (with a 'Temperatures...' button)
- Max Prop Delay (with a text input field and 'ns' unit)
- Max Frequency (with a text input field and 'MHz' unit)
- Max Current Usage (with a text input field and 'ma' unit)
- User 1 (with a dropdown menu and a text input field)
- User 2 (with a dropdown menu and a text input field)
- Max Devices: 20
- Available File: plsynlib.avl

Buttons: OK, Cancel, Help



The 'Select Device Templates' dialog box displays a list of device templates:

A100	MACH215
A153	MACH220
A173	MACH221
A253	MACH230
A273	MACH231
MACH110	MACH355
MACH111	MACH435
MACH111SP	MACH445
MACH120	MACH465
MACH130	MV192_104
MACH131	MV192_120
MACH210	MV192_160
MACH211	MV192_68
MACH211SP	MV256_104

Buttons: OK, Cancel, All, None

Use <CTRL-CLICK> to toggle single
Use <CTRL-DRAG> to toggle block selection



Fitting the Logic

Select the solution that best meets your requirements.

Run the PLSyn Fitter to find solutions based on your constraints. Solutions can be a single device or multiple devices with the same or different architectures.

PLSyn - [SA_ADC.sch]

File Edit Tools Window Help

Solutions

Solution	Device	Icc	Tmin	Price
1.	2 X P16V8A, P22V10	270ma	55ns	\$3.20
2.	P16V8A, P16R8, P22V10	280ma	55ns	\$3.22
3.	2 X P16R8, P22V10	290ma	55ns	\$3.24
4.	2 X P16V8A, P18V10	295ma	27ns	\$3.40
5.	P16V8A, P16R8, P18V10	305ma	33ns	\$3.42
6.	2 X P16R8, P18V10	315ma	33ns	\$3.44
7.	P16V8A, 2 X P22V10	270ma	55ns	\$4.45
8.	P16R8, 2 X P22V10	280ma	55ns	\$4.47
9.	P16V8A, P22V10, P18V10	295ma	55ns	\$4.65
10.	P16R8, P22V10, P18V10	305ma	55ns	\$4.67

Solution Detail

Device Name

PALCE16V8-25JC	C
PALCE16V8-25JC	C

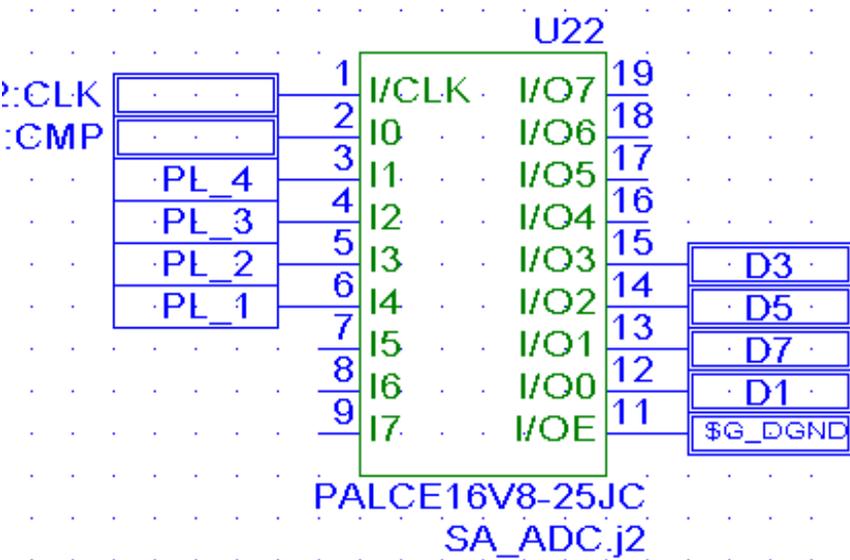
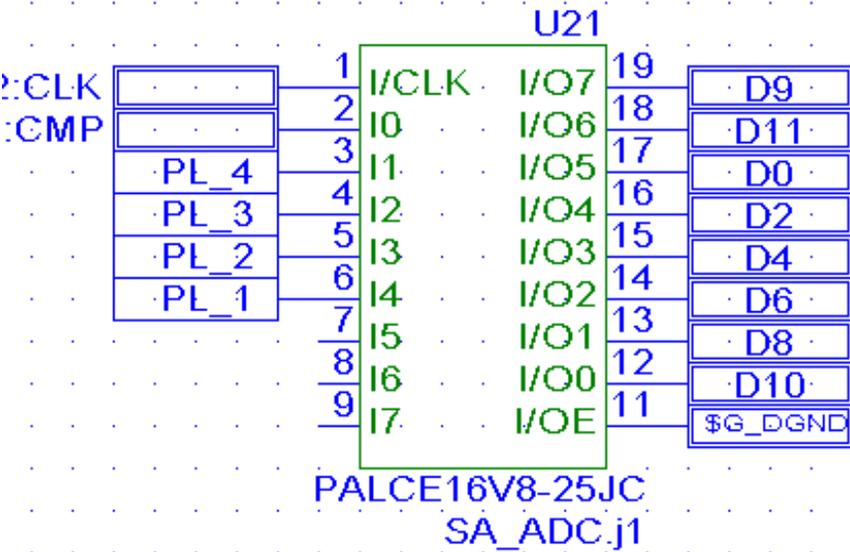
Select Device

Device Name	Mfg.	Fam.	Pkg.	Temp.	Icc	Tmin	Price	U1	U2
PALCE16V8-25JC	CYP	CMOS	JLCC	COM	90ma	27ns	\$0.65	0	0
PALCE16V8-25PC	CYP	CMOS	DIP	COM	55ma	27ns	\$0.65	0	0
PALCE16V8-15PC	CYP	CMOS	DIP	COM	90ma	22ns	\$0.70	0	0
PALCE16V8-15JC	CYP	CMOS	JLCC	COM	90ma	22ns	\$0.75	0	0
PALCE16V8L-25JC	CYP	CMOS	JLCC	COM	55ma	22ns	\$0.75	0	0
PALCE16V8-25PI	CYP	CMOS	DIP	EXT	130ma	27ns	\$0.80	0	0
PALCE16V8-25JI	CYP	CMOS	JLCC	EXT	130ma	27ns	\$0.85	0	0
PALCE16V8-15PI	CYP	CMOS	DIP	EXT	130ma	22ns	\$0.95	0	0
PALCE16V8H-25JC/4	AMD	CMOS	JLCC	COM	90ma	27ns	\$0.98	0	0
PALCE16V8H-25PC/4	AMD	CMOS	DIP	COM	90ma	27ns	\$0.98	0	0
ATF16V8B-15JC	ATM	CMOS	JLCC	COM	115ma	21ns	\$1.00	0	0

OK Cancel Help

Select the part(s) to use for the chosen solution.





Preparing for PCB Layout

Use PLSyn to update the schematic with the selected part(s).

When you create the PCB netlist for the system, the PLDs/CPLDs will be included.



MicroSim PLSyn

Bring accurate circuits to market faster!

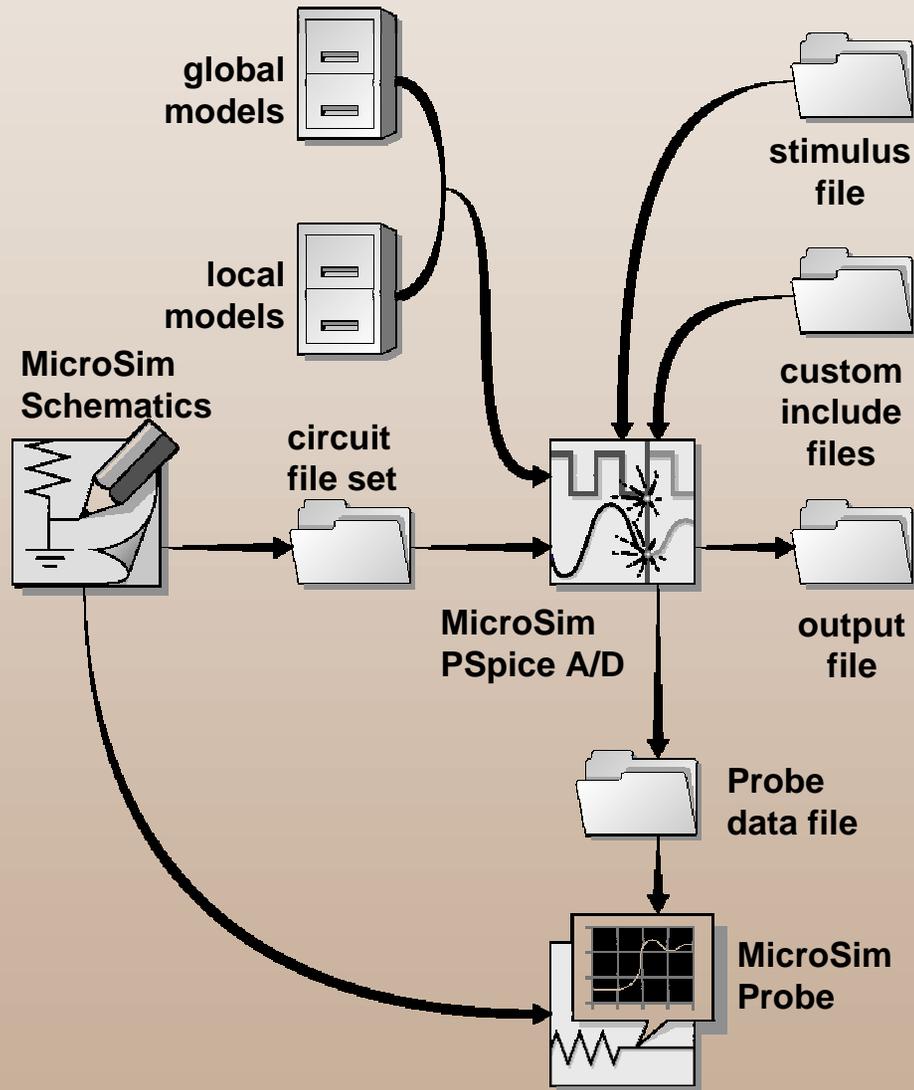
Only from
MicroSim

- ➔ Only PC-based tool that integrates PLDs and CPLDs with analog and discrete digital devices in a complete system design.
- ➔ Creates a list of device solutions to your logic design; you select the best solution.
- ➔ Integrated simulation: access both functional and timing analysis through Schematics.



click

Using MicroSim PSpice A/D



The Simulation Process:

- ① Create and prepare the schematic for simulation with MicroSim Schematics.
- ② Perform circuit simulation and analysis with PSpice.
- ③ View simulation results with Probe.



Simulating a Circuit with PSpice A/D

- ➔ **PSpice performs simulation and analysis by:**
 - ❶ **Interpreting the information for the circuit in the Schematics files.**
 - ❷ **Automatically running the simulation.**
 - ❸ **Producing the Probe data file and simulation output file.**
- ➔ **When simulating, the wire connections to the pins of parts shown in a schematic are transformed into electrical node connections to device terminals that are interpreted by PSpice.**



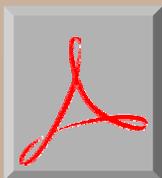
Displaying Simulation Results

Probe Data Files

- ★ The Probe data file contains simulation results that can be viewed and manipulated in Probe, MicroSim's graphical waveform analyzer application.
- ★ Probe reads the data and displays waveforms reflecting circuit response at marked nets, pins, and devices in your schematic or for output variables that you can specify in Probe.

Simulation Output Files

- ★ The simulation output file is an ASCII text file containing lists and tables describing the input circuit, the analysis directives, and the results of the specified simulations.



PSpice A/D
User's Guide

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Using MicroSim Schematics

- ➔ **Schematics is a front-end schematic capture program that you can use to:**



create and edit designs



create and edit symbols



create and edit hierarchical designs



prepare a design for simulation

- ➔ **Schematics has extensive symbol libraries and a fully integrated symbol editor for creating your own symbols or modifying existing symbols.**



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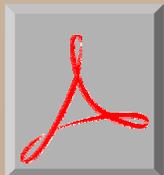
Starting a New Design



To start the schematic editor with an empty schematic page: from the Start menu, point to the MicroSim program group, then select Schematics.



If you already have Schematics running with another schematic displayed, click the New File button on the toolbar to start a new schematic.



**Schematics
User's Guide**

click



click

What's New in MicroSim Schematics

Design Journal:

- ★ Create a checkpoint of a design.
- ★ Select non-MicroSim files to save with design checkpoint.
- ★ Record notes with a checkpoint.
- ★ Restore a checkpoint.
- ★ Work on multiple design checkpoints simultaneously.

Hierarchical Block Creation:

- ★ Create a hierarchical block from an existing schematic.
- ★ Place pins automatically for each schematic port.
- ★ Accelerate bottom-up design and reduce errors that occur when manually placing pins.



What's New in MicroSim Schematics

Design Manager:

- ★ Create and manage workspaces for better design organization.
- ★ Archive (and restore) designs.
- ★ Create a copy of a design.
- ★ Graphically browse to see a design's components and dependencies.
- ★ Drag-and-drop design components between designs.
- ★ Localize design dependencies. (Creates a self-contained instance of a design.)
- ★ Provide context-sensitive Help.



What's New in MicroSim Schematics

Annotation Graphics:

- ★ Fill shapes for diodes, transistors, and other symbols.
- ★ Annotate the schematic with graphics as well as text.
- ★ Add notes to an area of the schematic.
- ★ Control graphic properties and text appearance.
- ★ Incorporate bitmap graphics, such as a company logo.
- ★ Create zoned borders.
- ★ Output DXF.

WYSIWYG Orthogonal Rubberbanding:

- ★ Connectivity Watcher.
- ★ Automatic Stair Stepping.
- ★ Pin-to-Pin Connections are rubberbanded.



What's New in MicroSim PSpice and PSpice A/D with Schematics

Design Journal:

- ★ Compare simulation results of different checkpoints (overlaid or in separate plots).
- ★ Display color-coded results in MicroSim Probe by design checkpoint.
- ★ See checkpoint and description properties of a trace in MicroSim Probe.

Device Noise Spectra:

- ★ View individual device noise contributions in MicroSim Probe. Data available include total noise contribution and the noise components of individual devices.



What's New in MicroSim PSpice and PSpice A/D with Schematics

Bias Point Display

- ★ Displays the latest set of bias point information (Small Signal Bias/DC Bias point or initial transient analysis) within MicroSim Schematics. The information available for display includes analog voltages and digital states on wires, and currents into devices into device pins for both simulation primitives and macro-models.
- ★ Supports user-definable options (display ON/OFF, color, position, and precision control of displayed data, etc., which become the default for subsequent sessions).
- ★ Locates the source of topology errors such as floating nodes.
- ★ Displayed values can be printed (as shown on schematic) for documentation purposes.



What's New in MicroSim PSpice and PSpice A/D with Schematics

Symbols from Models

- ★ Automatically generates symbols for the models extracted by MicroSim Parts.
- ★ Automatically generates the corresponding symbol libraries for simulation model libraries.
- ★ Automatically configures the newly created or updated symbol and model libraries for immediate use in MicroSim Schematics.
- ★ Bases the symbol generation on MicroSim's default symbol set or user-provided symbol set.
- ★ Generates symbols for analog, digital, or mixed-signal devices (both primitives and macro-models).



What's New in MicroSim PSpice and PSpice A/D with Schematics

BSIM3 V3 Built-In Model:

- ★ Support for the Berkeley BSIM3 V3 MOSFET model in MicroSim PSpice.

Device Equations Option:

- ★ Compiler manufacturer and version independence.
- ★ Device equations now in separately loaded DLL.



What's New in MicroSim PCBoards

Graphical Footprint Browser:

- ★ Graphical part browser in layout editor.
- ★ Graphical footprint browser in footprint editor.
- ★ Checks for floating copper.
- ★ Generated Autorouting Rules Report.

Interactive Netlist Read-In:

- ★ Netlist read-in and problem resolution.
- ★ Complete netlist read-in on first try with problem reporting.
- ★ Interactive problem resolution to correct database.

DXF Input and Output:

- ★ Imports and exports mechanical drawing files in DXF format.



What's New in MicroSim DesignLab

- ★ Design Journal
- ★ Design Manager
- ★ WYSIWYG Orthogonal Rubberbanding
- ★ Bias Point Display
- ★ Device Noise Spectra
- ★ Symbols from Models
- ★ BSIM3 V3 Built-In Model
- ★ Device Equations Option
- ★ Graphical Footprint Browser
- ★ Interactive Netlist Read-In
- ★ DXF Input and Output



What's New in MicroSim DesignLab

Simulate Multiple Xilinx FPGAs

- ★ Each FPGA is simply represented as a hierarchical block and can be connected to analog and discrete digital components or other FPGAs.
- ★ Each FPGA can be from a different family.
- ★ Allows multiple-FPGA designs to be in different stages of completion.

Import XNF

- ★ Allows simulation of any Xilinx FPGA within a mixed analog/digital circuit.
- ★ Pins are added to the block automatically.
- ★ Supports XNF (Xilinx Netlist Format, versions 5 and 6) file from any source such as from obsolete design tools, synthesis tools, etc.
- ★ Automatically uses post place and route timing information if present in the XNF file.

